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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,412	02/27/2004	Hajime Saiki	Q80149	4528

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EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,412	SAIKI ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *2 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of specie A1B2, claims 1, 3, 5 and 6 in the reply filed on August 3, 2005 is acknowledged.

Specification

2. The abstract of the disclosure is objected to because of inclusion of legal phraseology "comprising". The abstract should be in narrative form and should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full test for details.

Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 1, 3, 5 and 6 are objected to because of the following:

Regarding claim 1, "a conductor layer and a resin layer", line 2 and "an internal conductor layer" and "at least one of said resin layer", line, 10-11, are misguiding. For the examination purpose it is assumed that "an internal conductor layer" on line 10-11 is referring to "a conductor layer" on line 2, and "at least one of said resin layer" on line 10-11 if referring to "a resin layer" on line 2.

Claim 3 depend on claim 1 and inherit the same deficiency.

Regarding claim 5, the phrase "a core substrate including a through hole provided through an insulating substrate" is misguiding. It is unclear whether the

through hole is provided only in the insulating substrate or is also through the core substrate as a whole. Based on the figure and description, for the examination purpose, it is assumed that the through hole is through the core substrate as whole.

Further, a connection portion including **either**: "via conductors buried individually in said resin layer"; **or** "said via conductors and a third earthing conductor layer provided between the same resin layers as said transmission line and having no conduction to said transmission line" are two different limitations reading on two different species. The limitation "said via conductors and a third earthing conductor layer provided between the same resin layers as said transmission line and having no conduction to said transmission line" is not reading on the elected specie, therefore the claim with this alternate limitation is not considered. Only the first limitation is considered in applying the prior art.

Claim 6 depend on claim 5 and inherit the same deficiency. Further, **either** "a stacked via structure, in which a plurality of filled vias are concentrically contiguous to each other at a position avoiding that above said through hole", line 2-4; **or** "a structure, in which said third earthing conductor layer is connected between any contiguous ones of said filled vias in said stacked via structure is provided", line 5-7, are two different limitations reading on two different species. The limitation "a structure, in which said third earthing conductor layer is connected between any contiguous ones of said filled vias in said stacked via structure is provided", is not reading on the elected specie, therefore the claim with this alternate limitation is not considered. Only the first limitation is considered in applying the prior art.

The claims appear to be a literal translation into English from a foreign document.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, and 5, as best understood to the examiner, are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al., US Patent No. 4,963,697 (Peterson) in view of Kawasaki et al., US Patent No. 6,930,258 (Kawasaki).

Regarding claim 1, Peterson, in figure 1, discloses a wiring substrate, in which a wiring stacked portion including a conductor layer (one of the conductor layers 105) and a resin layer (one of the resin layers 101) is stacked on a principal face of a core substrate (102 with dielectric layer on top and bottom) including a substantially cylindrical through hole conductor (through hole in the core layer with plating) in a through hole extending there through, comprising: a cover-shaped conductor (conductor 105 on the through hole, see figure 1) portion covering an end face of said through hole just over a principal face of said core substrate and connected to said through hole conductor; and an internal conductor layer (one of the conductor layers 105, above the

one covering the through hole) provided in said wiring stacked portion and across at least one of said resin layer from said cover-shaped conductor layer, wherein a connection portion (via connecting the cover shaped conductor layer and the other conductor) composed of via conductors (via connecting the cover shaped conductor layer and the other conductor) buried in said resin layer brings said cover-shaped conductor portion and said internal conductor layer into conduction, and said via conductors composing said connection portion are provided not above said through hole (see figure 1).

Peterson does not disclose the filling material filling the hollow portion of said through hole.

Kawasaki, in figure 6, discloses a through hole (35) in the core substrate filled with a filling material (54) to have better strength of the via hole for enhanced reliability of the circuit board (column 5, line 12-27).

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to fill the through hole to have a better strength and enhanced reliability of the circuit board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Peterson with the through hole filled with a filling material in order to have the through hole with a better strength and enhanced reliability of the circuit board.

Regarding claim 3, the modified circuit board of Peterson discloses all the features of the claimed invention as applied to claim 1 above but does not disclose a distance from a center axis of said via conductor constructing said connection portion to an outer edge of said through hole is from 125 μm to 500 μm. However, the distance will be decided based on the routing of the conductor traces to optimize the space available to increase the trace density for connecting the components. Further, optimization of the available space will help in reducing the size of the circuit board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Peterson with a distance from a center axis of said via conductor constructing said connection portion to an outer edge of said through hole is from 125 μm to 500 μm to optimize the available space on the circuit board with better routing of the traces.

Regarding claim 5, Peterson in figure 1 discloses a wiring substrate comprising: a core substrate (102 with dielectric layer on top and bottom) including a through hole (through hole in the core layer with plating) provided through an insulating substrate, a substantially cylindrical through hole conductors provided on an inner circumference of said through hole (through hole in the core layer with **plating**); a first earthing conductor layer (one of the conductors 105 on the through hole, see figure 1) provided on at least one principal face of said core substrate and in a shape containing an end face of said through hole and having conduction to said through hole conductor; a plurality of resin layers (101) provided over said first earthing conductor layer; a transmission line

(second conductor from top layer on the left in figure 1) provided between any ones of said resin layers and positioned above said first earthing conductor layer; a second earthing conductor layer (first conductor layer below upper/top dielectric layer) provided over said resin layers and in a shape containing said transmission line; and a connection portion including via conductors (via connecting the conductors) buried individually in said resin layers; said via conductors being provided to bring said first earthing conductor layer and said second earthing conductor layer into conduction, wherein said via conductors to be connected to said first earthing conductor layer are positioned in said connection portion so as not to be above said through hole (see figure 1, vias are not formed on the through hole).

Peterson does not disclose the filling material filling the hollow portion of said through hole.

Kawasaki, in figure 6, discloses a through hole (35) in the core substrate filled with a filling material (54) to have better strength of the via hole for enhanced reliability of the circuit board (column 5, line 12-27).

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to fill the through hole to have a better strength and enhanced reliability of the circuit board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Peterson with the through hole filled with a filling material, as taught by Kawasaki, in order to have the through hole with a better strength and enhanced reliability of the circuit board.

6. Claim 6, as best understood to the examiner, is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Peterson and Kawasaki, as applied to claim 5 above, and further in view of Shimada et al., US Patent No. 6,353,189 (Shimada).

Regarding claim 6, the combination of Peterson and Kawasaki discloses all the features of the claimed invention as applied to claim 5 above, but does not discloses the stacked via structure, in which a plurality of filled vias are concentrically contiguous to each other at a position avoiding that above said through hole. Peterson discloses the stacked via structure as shown in figure 1, avoiding the through hole, but dose not disclose them in concentric form.

Shimada, in figure 1, discloses a wiring board with via 7a-7b, formed in the concentric form for providing shielding to the transmission line 1. Further, it can be seen from the figure that concentric via will occupy less space than that of nonconcentric via.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified circuit board of Peterson with the filled via concentric to each other, as taught by Shimada, in order to provide better shielding and occupy less space on the circuit board.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Echigo et al., US Patent No. 6,274,821, in figure 1, discloses a circuit board with a through hole (4) in the core substrate (1) with a cover on the through hole and via holes not formed directly on the through hole.

Enomoto et al., US Patent No. 6,586,686,in figure 1, discloses circuit board with a through hole (24) in the core substrate (20) and concentric filled via holes (36c-36d) not formed directly on the through hole.

Hayakawa et al., US Patent No. 4,383,363, in figure 2 (c) disclose a through hole in substrate (24) covered with conductive layers (30,32).

Ishikawa et al., US Patent No. 5,243,142, in figure 3, discloses a circuit board with through hole (5) in core substrate (1) with cover layer (6).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IB Patel

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
September 3, 2005